Proving that the cache works: Running the loop for 12 iterations instead of 1,000,000

**MemGen1 output addresses:**

addr 0: 0

addr 1: 1

addr 2: 2

addr 3: 3

addr 4: 4

addr 5: 5

addr 6: 6

addr 7: 7

addr 8: 8

addr 9: 9

addr 10: 10

addr 11: 11

*Experiment 1: Direct Mapping:*

First:

The cache size =64, and varying line size from 4 to 128 bytes, steps of power 2

1. cache size =64; line size 4 bytes:

2 offset bits; 14 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a compulsory miss

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a compulsory miss

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= ¼=0.25

1. cache size =64; line size 8 bytes:

2 offset byte bits; 1 bit for word offset; 13 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a compulsory miss

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 2/12= 0.16667

1. cache size =64; line size 16 bytes:

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 32 bytes:

2 offset byte bits; 3 bit for word offset; 11 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 64 bytes:

2 offset byte bits; 4 bit for word offset; 10 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 128 bytes:

2 offset byte bits; 5 bit for word offset; 9 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

Here it is apparent how increasing the line size will decrease the miss rate

Second: Cache size varies from 1 to, steps of power 2, line size 16 bytes

1. Line size =16 bytes; Cache size= 1 KBs

2 offset byte bits; 2 bit for word offset; 6 bits for index; 22 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 2 KBs

2 offset byte bits; 2 bit for word offset; 7 bits for index; 21 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 4 KBs

2 offset byte bits; 2 bit for word offset; 8 bits for index; 20 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 8 KBs

2 offset byte bits; 2 bit for word offset; 9 bits for index; 19 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 16 KBs

2 offset byte bits; 2 bit for word offset; 10 bits for index; 18 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 32 KBs

2 offset byte bits; 2 bit for word offset; 11 bits for index; 17 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 64 KBs

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

**MemGen2 output addresses:**

addr 0: 95291

addr 1: 41855

addr 2: 127388

addr 3: 87463

addr 4: 45196

addr 5: 35654

addr 6: 121437

addr 7: 119120

addr 8: 99577

addr 9: 56653

addr 10: 23189

addr 11: 18776

*Experiment 1: Direct Mapping*:

First:

The cache size =64, and varying line size from 4 to 128 bytes, steps of power 2

1. cache size =64; line size 4 bytes:

2 offset bits; 14 bits for index; 16 bits for tag

Address (10 1110100001110 11)2 will have a compulsory miss

Address (01 0100011011111 11)2 will have a compulsory miss

Address (11 1110001100111 00)2 will have a compulsory miss

Address (10 1010101101001 11)2 will have a compulsory miss

Address (01 0110000100011 00)2 will have a compulsory miss

Address (01 0001011010001 10)2 will have a compulsory miss

Address (01 1101101001011 10)2 will have a compulsory miss

Address (11 1010001010100 00)2 will have a compulsory miss

Address (11 0000100111110 01)2 will have a compulsory miss

Address (01 1011101010011 01)2 will have a compulsory miss

Address (00 1011010100101 01)2 will have a compulsory miss

Address (00 1001001010110 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 8 bytes:

2 offset byte bits; 1 bit for word offset; 13 bits for index; 16 bits for tag

Address (10 111010000111 0 11)2 will have a compulsory miss

Address (01 010001101111 1 11)2 will have a compulsory miss

Address (11 111000110011 1 00)2 will have a compulsory miss

Address (10 101010110100 1 11)2 will have a compulsory miss

Address (01 011000010001 1 00)2 will have a compulsory miss

Address (01 000101101000 1 10)2 will have a compulsory miss

Address (01 110110100101 1 10)2 will have a compulsory miss

Address (11 101000101010 0 00)2 will have a compulsory miss

Address (11 000010011111 0 01)2 will have a compulsory miss

Address (01 101110101001 1 01)2 will have a compulsory miss

Address (00 101101010010 1 01)2 will have a compulsory miss

Address (00 100100101011 0 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 16 bytes:

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (10 11101000011 10 11)2 will have a compulsory miss

Address (01 01000110111 11 11)2 will have a compulsory miss

Address (11 11100011001 11 00)2 will have a compulsory miss

Address (10 10101011010 01 11)2 will have a compulsory miss

Address (01 01100001000 11 00)2 will have a compulsory miss

Address (01 00010110100 01 10)2 will have a compulsory miss

Address (01 11011010010 11 10)2 will have a compulsory miss

Address (11 10100010101 00 00)2 will have a compulsory miss

Address (11 00001001111 10 01)2 will have a compulsory miss

Address (01 10111010100 11 01)2 will have a compulsory miss

Address (00 10110101001 01 01)2 will have a compulsory miss

Address (00 10010010101 10 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 32 bytes:

2 offset byte bits; 3 bit for word offset; 11 bits for index; 16 bits for tag

Address (10 1110100001 110 11)2 will have a compulsory miss

Address (01 0100011011 111 11)2 will have a compulsory miss

Address (11 1110001100 111 00)2 will have a compulsory miss

Address (10 1010101101 001 11)2 will have a compulsory miss

Address (01 0110000100 011 00)2 will have a compulsory miss

Address (01 0001011010 001 10)2 will have a compulsory miss

Address (01 1101101001 011 10)2 will have a compulsory miss

Address (11 1010001010 100 00)2 will have a compulsory miss

Address (11 0000100111 110 01)2 will have a compulsory miss

Address (01 1011101010 011 01)2 will have a compulsory miss

Address (00 1011010100 101 01)2 will have a compulsory miss

Address (00 1001001010 110 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 64 bytes:

2 offset byte bits; 4 bit for word offset; 10 bits for index; 16 bits for tag

Address (10 111010000 1110 11)2 will have a compulsory miss

Address (01 010001101 1111 11)2 will have a compulsory miss

Address (11 111000110 0111 00)2 will have a compulsory miss

Address (10 101010110 1001 11)2 will have a compulsory miss

Address (01 011000010 0011 00)2 will have a compulsory miss

Address (01 000101101 0001 10)2 will have a compulsory miss

Address (01 110110100 1011 10)2 will have a compulsory miss

Address (11 101000101 0100 00)2 will have a compulsory miss

Address (11 000010011 1110 01)2 will have a compulsory miss

Address (01 101110101 0011 01)2 will have a compulsory miss

Address (00 101101010 0101 01)2 will have a compulsory miss

Address (00 100100101 0110 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 128 bytes:

2 offset byte bits; 5 bit for word offset; 9 bits for index; 16 bits for tag

Address (10 11101000 01110 11)2 will have a compulsory miss

Address (01 01000110 11111 11)2 will have a compulsory miss

Address (11 11100011 00111 00)2 will have a compulsory miss

Address (10 10101011 01001 11)2 will have a compulsory miss

Address (01 01100001 00011 00)2 will have a compulsory miss

Address (01 00010110 10001 10)2 will have a compulsory miss

Address (01 11011010 01011 10)2 will have a compulsory miss

Address (11 10100010 10100 00)2 will have a compulsory miss

Address (11 00001001 11110 01)2 will have a compulsory miss

Address (01 10111010 10011 01)2 will have a compulsory miss

Address (00 10110101 00101 01)2 will have a compulsory miss

Address (00 10010010 10110 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

Second: Cache size varies from 1 to, steps of power 2, line size 16 bytes

1. Line size =16 bytes; Cache size= 1 KBs

2 offset byte bits; 2 bit for word offset; 6 bits for index; 22 bits for tag

Address (1011101 000011 10 11)2 will have a compulsory miss

Address (0101000 110111 11 11)2 will have a compulsory miss

Address (1111100 011001 11 00)2 will have a compulsory miss

Address (1010101 011010 01 11)2 will have a compulsory miss

Address (0101100 001000 11 00)2 will have a compulsory miss

Address (0100010 110100 01 10)2 will have a compulsory miss

Address (0111011 010010 11 10)2 will have a compulsory miss

Address (1110100 010101 00 00)2 will have a compulsory miss

Address (1100001 001111 10 01)2 will have a compulsory miss

Address (0110111 010100 11 01)2 will have a compulsory miss

Address (0010110 101001 01 01)2 will have a compulsory miss

Address (0010010 010101 10 00)2 will have a conflict miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 2 KBs

2 offset byte bits; 2 bit for word offset; 7 bits for index; 21 bits for tag

Address (101110 1000011 10 11)2 will have a compulsory miss

Address (010100 0110111 11 11)2 will have a compulsory miss

Address (111110 0011001 11 00)2 will have a compulsory miss

Address (101010 1011010 01 11)2 will have a compulsory miss

Address (010110 0001000 11 00)2 will have a compulsory miss

Address (010001 0110100 01 10)2 will have a compulsory miss

Address (011101 1010010 11 10)2 will have a compulsory miss

Address (111010 0010101 00 00)2 will have a compulsory miss

Address (110000 1001111 10 01)2 will have a compulsory miss

Address (011011 1010100 11 01)2 will have a compulsory miss

Address (001011 0101001 01 01)2 will have a compulsory miss

Address (001001 0010101 10 00)2 will have a conflict miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 4 KBs

2 offset byte bits; 2 bit for word offset; 8 bits for index; 20 bits for tag

Address (10111 01000011 10 11)2 will have a compulsory miss

Address (01010 00110111 11 11)2 will have a compulsory miss

Address (11111 00011001 11 00)2 will have a compulsory miss

Address (10101 01011010 01 11)2 will have a compulsory miss

Address (01011 00001000 11 00)2 will have a compulsory miss

Address (01000 10110100 01 10)2 will have a compulsory miss

Address (01110 11010010 11 10)2 will have a compulsory miss

Address (11101 00010101 00 00)2 will have a compulsory miss

Address (11000 01001111 10 01)2 will have a compulsory miss

Address (01101 11010100 11 01)2 will have a compulsory miss

Address (00101 10101001 01 01)2 will have a compulsory miss

Address (00100 10010101 10 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 8 KBs

2 offset byte bits; 2 bit for word offset; 9 bits for index; 19 bits for tag

Address (1011 101000011 10 11)2 will have a compulsory miss

Address (0101 000110111 11 11)2 will have a compulsory miss

Address (1111 100011001 11 00)2 will have a compulsory miss

Address (1010 101011010 01 11)2 will have a compulsory miss

Address (0101 100001000 11 00)2 will have a compulsory miss

Address (0100 010110100 01 10)2 will have a compulsory miss

Address (0111 011010010 11 10)2 will have a compulsory miss

Address (1110 100010101 00 00)2 will have a compulsory miss

Address (1100 001001111 10 01)2 will have a compulsory miss

Address (0110 111010100 11 01)2 will have a compulsory miss

Address (0010 110101001 01 01)2 will have a compulsory miss

Address (0010 010010101 10 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 16 KBs

2 offset byte bits; 2 bit for word offset; 10 bits for index; 18 bits for tag

Address (101 1101000011 10 11)2 will have a compulsory miss

Address (010 1000110111 11 11)2 will have a compulsory miss

Address (111 1100011001 11 00)2 will have a compulsory miss

Address (101 0101011010 01 11)2 will have a compulsory miss

Address (010 1100001000 11 00)2 will have a compulsory miss

Address (010 0010110100 01 10)2 will have a compulsory miss

Address (011 1011010010 11 10)2 will have a compulsory miss

Address (111 0100010101 00 00)2 will have a compulsory miss

Address (110 0001001111 10 01)2 will have a compulsory miss

Address (011 0111010100 11 01)2 will have a compulsory miss

Address (001 0110101001 01 01)2 will have a compulsory miss

Address (001 0010010101 10 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 32 KBs

2 offset byte bits; 2 bit for word offset; 11 bits for index; 17 bits for tag

Address (10 11101000011 10 11)2 will have a compulsory miss

Address (01 01000110111 11 11)2 will have a compulsory miss

Address (11 11100011001 11 00)2 will have a compulsory miss

Address (10 10101011010 01 11)2 will have a compulsory miss

Address (01 01100001000 11 00)2 will have a compulsory miss

Address (01 00010110100 01 10)2 will have a compulsory miss

Address (01 11011010010 11 10)2 will have a compulsory miss

Address (11 10100010101 00 00)2 will have a compulsory miss

Address (11 00001001111 10 01)2 will have a compulsory miss

Address (01 10111010100 11 01)2 will have a compulsory miss

Address (00 10110101001 01 01)2 will have a compulsory miss

Address (00 10010010101 10 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 64 KBs

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (1 011101000011 10 11)2 will have a compulsory miss

Address (0 101000110111 11 11)2 will have a compulsory miss

Address (1 111100011001 11 00)2 will have a compulsory miss

Address (1 010101011010 01 11)2 will have a compulsory miss

Address (0 101100001000 11 00)2 will have a compulsory miss

Address (0 100010110100 01 10)2 will have a compulsory miss

Address (0 111011010010 11 10)2 will have a compulsory miss

Address (1 110100010101 00 00)2 will have a compulsory miss

Address (1 100001001111 10 01)2 will have a compulsory miss

Address (0 110111010100 11 01)2 will have a compulsory miss

Address (0 010110101001 01 01)2 will have a compulsory miss

Address (0 010010010101 10 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

**MemGen3 output addresses:**

addr 0: 53810273

addr 1: 37943413

addr 2: 6924328

addr 3: 27377853

addr 4: 22746943

addr 5: 34583200

addr 6: 45979746

addr 7: 56531887

addr 8: 40872586

addr 9: 65548770

addr 10: 23302519

addr 11: 64490723

*Experiment 1: Direct Mapping:*

First:

The cache size =64, and varying line size from 4 to 128 bytes, steps of power 2

1. cache size =64; line size 4 bytes:

2 offset bits; 14 bits for index; 16 bits for tag

Address (1100110101 00010100011000 01)2 will have a compulsory miss

Address (1001000010 11111000011101 01)2 will have a compulsory miss

Address (0001101001 10101000001010 00)2 will have a compulsory miss

Address (0110100001 11000000101111 01)2 will have a compulsory miss

Address (0101011011 00010111001111 11)2 will have a compulsory miss

Address (1000001111 10110010101000 00)2 will have a compulsory miss

Address (1010111101 10011000011000 10)2 will have a compulsory miss

Address (1101011110 10011011101011 11)2 will have a compulsory miss

Address (1001101111 10101010100010 10)2 will have a compulsory miss

Address (1111101000 00110001111000 10)2 will have a compulsory miss

Address (0101100011 10010001011101 11)2 will have a compulsory miss

Address (1111011000 00001100111000 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 8 bytes:

2 offset byte bits; 1 bit for word offset; 13 bits for index; 16 bits for tag

Address (1100110101 0001010001100 0 01)2 will have a compulsory miss

Address (1001000010 1111100001110 1 01)2 will have a compulsory miss

Address (0001101001 1010100000101 0 00)2 will have a compulsory miss

Address (0110100001 1100000010111 1 01)2 will have a compulsory miss

Address (0101011011 0001011100111 1 11)2 will have a compulsory miss

Address (1000001111 1011001010100 0 00)2 will have a compulsory miss

Address (1010111101 1001100001100 0 10)2 will have a compulsory miss

Address (1101011110 1001101110101 1 11)2 will have a compulsory miss

Address (1001101111 1010101010001 0 10)2 will have a compulsory miss

Address (1111101000 0011000111100 0 10)2 will have a compulsory miss

Address (0101100011 1001000101110 1 11)2 will have a compulsory miss

Address (1111011000 0000110011100 0 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 16 bytes:

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (1100110101 000101000110 00 01)2 will have a compulsory miss

Address (1001000010 111110000111 01 01)2 will have a compulsory miss

Address (0001101001 101010000010 10 00)2 will have a compulsory miss

Address (0110100001 110000001011 11 01)2 will have a compulsory miss

Address (0101011011 000101110011 11 11)2 will have a compulsory miss

Address (1000001111 101100101010 00 00)2 will have a compulsory miss

Address (1010111101 100110000110 00 10)2 will have a compulsory miss

Address (1101011110 100110111010 11 11)2 will have a compulsory miss

Address (1001101111 101010101000 10 10)2 will have a compulsory miss

Address (1111101000 001100011110 00 10)2 will have a compulsory miss

Address (0101100011 100100010111 01 11)2 will have a compulsory miss

Address (1111011000 000011001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 32 bytes:

2 offset byte bits; 3 bit for word offset; 11 bits for index; 16 bits for tag

Address (1100110101 00010100011 000 01)2 will have a compulsory miss

Address (1001000010 11111000011 101 01)2 will have a compulsory miss

Address (0001101001 10101000001 010 00)2 will have a compulsory miss

Address (0110100001 11000000101 111 01)2 will have a compulsory miss

Address (0101011011 00010111001 111 11)2 will have a compulsory miss

Address (1000001111 10110010101 000 00)2 will have a compulsory miss

Address (1010111101 10011000011 000 10)2 will have a compulsory miss

Address (1101011110 10011011101 011 11)2 will have a compulsory miss

Address (1001101111 10101010100 010 10)2 will have a compulsory miss

Address (1111101000 00110001111 000 10)2 will have a compulsory miss

Address (0101100011 10010001011 101 11)2 will have a compulsory miss

Address (1111011000 00001100111 000 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 64 bytes:

2 offset byte bits; 4 bit for word offset; 10 bits for index; 16 bits for tag

Address (1100110101 0001010001 1000 01)2 will have a compulsory miss

Address (1001000010 1111100001 1101 01)2 will have a compulsory miss

Address (0001101001 1010100000 1010 00)2 will have a compulsory miss

Address (0110100001 1100000010 1111 01)2 will have a compulsory miss

Address (0101011011 0001011100 1111 11)2 will have a compulsory miss

Address (1000001111 1011001010 1000 00)2 will have a compulsory miss

Address (1010111101 1001100001 1000 10)2 will have a compulsory miss

Address (1101011110 1001101110 1011 11)2 will have a compulsory miss

Address (1001101111 1010101010 0010 10)2 will have a compulsory miss

Address (1111101000 0011000111 1000 10)2 will have a compulsory miss

Address (0101100011 1001000101 1101 11)2 will have a compulsory miss

Address (1111011000 0000110011 1000 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 128 bytes:

2 offset byte bits; 5 bit for word offset; 9 bits for index; 16 bits for tag

Address (1100110101 000101000 11000 01)2 will have a compulsory miss

Address (1001000010 111110000 11101 01)2 will have a compulsory miss

Address (0001101001 101010000 01010 00)2 will have a compulsory miss

Address (0110100001 110000001 01111 01)2 will have a compulsory miss

Address (0101011011 000101110 01111 11)2 will have a compulsory miss

Address (1000001111 101100101 01000 00)2 will have a compulsory miss

Address (1010111101 100110000 11000 10)2 will have a compulsory miss

Address (1101011110 100110111 01011 11)2 will have a compulsory miss

Address (1001101111 101010101 00010 10)2 will have a compulsory miss

Address (1111101000 001100011 11000 10)2 will have a compulsory miss

Address (0101100011 100100010 11101 11)2 will have a compulsory miss

Address (1111011000 000011001 11000 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

Second: Cache size varies from 1 to, steps of power 2, line size 16 bytes

1. Line size =16 bytes; Cache size= 1 KBs

2 offset byte bits; 2 bit for word offset; 6 bits for index; 22 bits for tag

Address (1100110101000101 000110 00 01)2 will have a compulsory miss

Address (1001000010111110 000111 01 01)2 will have a compulsory miss

Address (0001101001101010 000010 10 00)2 will have a compulsory miss

Address (0110100001110000 001011 11 01)2 will have a compulsory miss

Address (0101011011000101 110011 11 11)2 will have a compulsory miss

Address (1000001111101100 101010 00 00)2 will have a compulsory miss

Address (1010111101100110 000110 00 10)2 will have a conflict miss

Address (1101011110100110 111010 11 11)2 will have a compulsory miss

Address (1001101111101010 101000 10 10)2 will have a compulsory miss

Address (1111101000001100 011110 00 10)2 will have a compulsory miss

Address (0101100011100100 010111 01 11)2 will have a compulsory miss

Address (1111011000000011 001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

(Due to the small size of the cache, the possibility of conflict misses will be so high (several addresses are highly probable to be mapped into the same cache address)

1. Line size =16 bytes; Cache size= 2 KBs

2 offset byte bits; 2 bit for word offset; 7 bits for index; 21 bits for tag

Address (110011010100010 1000110 00 01)2 will have a compulsory miss

Address (100100001011111 0000111 01 01)2 will have a compulsory miss

Address (000110100110101 0000010 10 00)2 will have a compulsory miss

Address (011010000111000 0001011 11 01)2 will have a compulsory miss

Address (010101101100010 1110011 11 11)2 will have a compulsory miss

Address (100000111110110 0101010 00 00)2 will have a compulsory miss

Address (101011110110011 0000110 00 10)2 will have a compulsory miss

Address (110101111010011 0111010 11 11)2 will have a compulsory miss

Address (100110111110101 0101000 10 10)2 will have a compulsory miss

Address (111110100000110 0011110 00 10)2 will have a compulsory miss

Address (010110001110010 0010111 01 11)2 will have a compulsory miss

Address (111101100000001 1001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

(Although we use here a slightly larger cache, the possibility of conflict misses will be still high, but it will be less a little bit than before (several addresses are highly probable to be mapped into the same cache address), while compulsory misses will be higher a little bit because we now have 2^7 lines instead of 2^6.

1. Line size =16 bytes; Cache size= 4 KBs

2 offset byte bits; 2 bit for word offset; 8 bits for index; 20 bits for tag

Address (11001101010001 01000110 00 01)2 will have a compulsory miss

Address (10010000101111 10000111 01 01)2 will have a compulsory miss

Address (00011010011010 10000010 10 00)2 will have a compulsory miss

Address (01101000011100 00001011 11 01)2 will have a compulsory miss

Address (01010110110001 01110011 11 11)2 will have a compulsory miss

Address (10000011111011 00101010 00 00)2 will have a compulsory miss

Address (10101111011001 10000110 00 10)2 will have a compulsory miss

Address (11010111101001 10111010 11 11)2 will have a compulsory miss

Address (10011011111010 10101000 10 10)2 will have a compulsory miss

Address (11111010000011 00011110 00 10)2 will have a compulsory miss

Address (01011000111001 00010111 01 11)2 will have a compulsory miss

Address (11110110000000 11001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 8 KBs

2 offset byte bits; 2 bit for word offset; 9 bits for index; 19 bits for tag

Address (1100110101000 101000110 00 01)2 will have a compulsory miss

Address (1001000010111 110000111 01 01)2 will have a compulsory miss

Address (0001101001101 010000010 10 00)2 will have a compulsory miss

Address (0110100001110 000001011 11 01)2 will have a compulsory miss

Address (0101011011000 101110011 11 11)2 will have a compulsory miss

Address (1000001111101 100101010 00 00)2 will have a compulsory miss

Address (1010111101100 110000110 00 10)2 will have a compulsory miss

Address (1101011110100 110111010 11 11)2 will have a compulsory miss

Address (1001101111101 010101000 10 10)2 will have a compulsory miss

Address (1111101000001 100011110 00 10)2 will have a compulsory miss

Address (0101100011100 100010111 01 11)2 will have a compulsory miss

Address (1111011000000 011001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 16 KBs

2 offset byte bits; 2 bit for word offset; 10 bits for index; 18 bits for tag

Address (110011010100 0101000110 00 01)2 will have a compulsory miss

Address (100100001011 1110000111 01 01)2 will have a compulsory miss

Address (000110100110 1010000010 10 00)2 will have a compulsory miss

Address (011010000111 0000001011 11 01)2 will have a compulsory miss

Address (010101101100 0101110011 11 11)2 will have a compulsory miss

Address (100000111110 1100101010 00 00)2 will have a compulsory miss

Address (101011110110 0110000110 00 10)2 will have a compulsory miss

Address (110101111010 0110111010 11 11)2 will have a compulsory miss

Address (100110111110 1010101000 10 10)2 will have a compulsory miss

Address (111110100000 1100011110 00 10)2 will have a compulsory miss

Address (010110001110 0100010111 01 11)2 will have a compulsory miss

Address (111101100000 0011001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 32 KBs

2 offset byte bits; 2 bit for word offset; 11 bits for index; 17 bits for tag

Address (11001101010 00101000110 00 01)2 will have a compulsory miss

Address (10010000101 11110000111 01 01)2 will have a compulsory miss

Address (00011010011 01010000010 10 00)2 will have a compulsory miss

Address (01101000011 10000001011 11 01)2 will have a compulsory miss

Address (01010110110 00101110011 11 11)2 will have a compulsory miss

Address (10000011111 01100101010 00 00)2 will have a compulsory miss

Address (10101111011 00110000110 00 10)2 will have a compulsory miss

Address (11010111101 00110111010 11 11)2 will have a compulsory miss

Address (10011011111 01010101000 10 10)2 will have a compulsory miss

Address (11111010000 01100011110 00 10)2 will have a compulsory miss

Address (01011000111 00100010111 01 11)2 will have a compulsory miss

Address (11110110000 00011001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 64 KBs

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (1100110101 000101000110 00 01)2 will have a compulsory miss

Address (1001000010 111110000111 01 01)2 will have a compulsory miss

Address (0001101001 101010000010 10 00)2 will have a compulsory miss

Address (0110100001 110000001011 11 01)2 will have a compulsory miss

Address (0101011011 000101110011 11 11)2 will have a compulsory miss

Address (1000001111 101100101010 00 00)2 will have a compulsory miss

Address (1010111101 100110000110 00 10)2 will have a compulsory miss

Address (1101011110 100110111010 11 11)2 will have a compulsory miss

Address (1001101111 101010101000 10 10)2 will have a compulsory miss

Address (1111101000 001100011110 00 10)2 will have a compulsory miss

Address (0101100011 100100010111 01 11)2 will have a compulsory miss

Address (1111011000 000011001110 00 11)2 will have a compulsory miss

So miss ratio= 12/12= 1

We can see from the second case on, the number of cache conflict misses will be less and less as we increase the number of lines in the cache since the number of memory addresses which are about to be mapped into the same cache address will decrease. On the other hand, the number of compulsory misses will increase as long as we do increase the number of lines in the cache. This fact keeps the miss rate almost the same no matter how much we increase or decrease the cache size; however, it should lessen the miss rate on the long run when having 1,000,000 iterations.

**MemGen4 output addresses:**

addr 0: 0

addr 1: 1

addr 2: 2

addr 3: 3

addr 4: 4

addr 5: 5

addr 6: 6

addr 7: 7

addr 8: 8

addr 9: 9

addr 10: 10

addr 11: 11

*Experiment 1: Direct Mapping:*

First:

The cache size =64, and varying line size from 4 to 128 bytes, steps of power 2

1. cache size =64; line size 4 bytes:

2 offset bits; 14 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a compulsory miss

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a compulsory miss

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= ¼=0.25

1. cache size =64; line size 8 bytes:

2 offset byte bits; 1 bit for word offset; 13 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a compulsory miss

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 2/12= 0.16667

1. cache size =64; line size 16 bytes:

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 32 bytes:

2 offset byte bits; 3 bit for word offset; 11 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 64 bytes:

2 offset byte bits; 4 bit for word offset; 10 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 128 bytes:

2 offset byte bits; 5 bit for word offset; 9 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

Second: Cache size varies from 1 to, steps of power 2, line size 16 bytes

1. Line size =16 bytes; Cache size= 1 KBs

2 offset byte bits; 2 bit for word offset; 6 bits for index; 22 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 2 KBs

2 offset byte bits; 2 bit for word offset; 7 bits for index; 21 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 4 KBs

2 offset byte bits; 2 bit for word offset; 8 bits for index; 20 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 8 KBs

2 offset byte bits; 2 bit for word offset; 9 bits for index; 19 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 16 KBs

2 offset byte bits; 2 bit for word offset; 10 bits for index; 18 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 32 KBs

2 offset byte bits; 2 bit for word offset; 11 bits for index; 17 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 64 KBs

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

**MemGen5 output addresses:**

addr 0: 0

addr 1: 1

addr 2: 2

addr 3: 3

addr 4: 4

addr 5: 5

addr 6: 6

addr 7: 7

addr 8: 8

addr 9: 9

addr 10: 10

addr 11: 11

*Experiment 1: Direct Mapping:*

First:

The cache size =64, and varying line size from 4 to 128 bytes, steps of power 2

1. cache size =64; line size 4 bytes:

2 offset bits; 14 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a compulsory miss

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a compulsory miss

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= ¼=0.25

1. cache size =64; line size 8 bytes:

2 offset byte bits; 1 bit for word offset; 13 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a compulsory miss

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 2/12= 0.16667

1. cache size =64; line size 16 bytes:

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 32 bytes:

2 offset byte bits; 3 bit for word offset; 11 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 64 bytes:

2 offset byte bits; 4 bit for word offset; 10 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. cache size =64; line size 128 bytes:

2 offset byte bits; 5 bit for word offset; 9 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

Second: Cache size varies from 1 to, steps of power 2, line size 16 bytes

1. Line size =16 bytes; Cache size= 1 KBs

2 offset byte bits; 2 bit for word offset; 6 bits for index; 22 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 2 KBs

2 offset byte bits; 2 bit for word offset; 7 bits for index; 21 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 4 KBs

2 offset byte bits; 2 bit for word offset; 8 bits for index; 20 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 8 KBs

2 offset byte bits; 2 bit for word offset; 9 bits for index; 19 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 16 KBs

2 offset byte bits; 2 bit for word offset; 10 bits for index; 18 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 32 KBs

2 offset byte bits; 2 bit for word offset; 11 bits for index; 17 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

1. Line size =16 bytes; Cache size= 64 KBs

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (0000)2 will have a compulsory miss

Address (0001)2 will have a hit

Address (0010)2 will have a hit

Address (0011)2 will have a hit

Address (0100)2 will have a hit

Address (0101)2 will have a hit

Address (0110)2 will have a hit

Address (0111)2 will have a hit

Address (1000)2 will have a hit

Address (1001)2 will have a hit

Address (1010)2 will have a hit

Address (1011)2 will have a hit

So miss ratio= 1/12= 0.08333

**MemGen6 output addresses:**

ddr 0: 256

addr 1: 512

addr 2: 768

addr 3: 1024

addr 4: 1280

addr 5: 1536

addr 6: 1792

addr 7: 2048

addr 8: 2304

addr 9: 2560

addr 10: 2816

addr 11: 3072

*Experiment 1: Direct Mapping:*

First:

The cache size =64, and varying line size from 4 to 128 bytes, steps of power 2

1. cache size =64; line size 4 bytes:

2 offset bits; 14 bits for index; 16 bits for tag

Address (00000001000000 00)2 will have a compulsory miss

Address (00000010000000 00)2 will have a compulsory miss

Address (00000011000000 00)2 will have a compulsory miss

Address (00000100000000 00)2 will have a compulsory miss

Address (00000101000000 00)2 will have a compulsory miss

Address (00000110000000 00)2 will have a compulsory miss

Address (00000111000000 00)2 will have a compulsory miss

Address (00001000000000 00)2 will have a compulsory miss

Address (00001001000000 00)2 will have a compulsory miss

Address (00001010000000 00)2 will have a compulsory miss

Address (00001011000000 00)2 will have a compulsory miss

Address (00001100000000 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 8 bytes:

2 offset byte bits; 1 bit for word offset; 13 bits for index; 16 bits for tag

Address (0000000100000 0 00)2 will have a compulsory miss

Address (0000001000000 0 00)2 will have a compulsory miss

Address (0000001100000 0 00)2 will have a compulsory miss

Address (0000010000000 0 00)2 will have a compulsory miss

Address (0000010100000 0 00)2 will have a compulsory miss

Address (0000011000000 0 00)2 will have a compulsory miss

Address (0000011100000 0 00)2 will have a compulsory miss

Address (0000100000000 0 00)2 will have a compulsory miss

Address (0000100100000 0 00)2 will have a compulsory miss

Address (0000101000000 0 00)2 will have a compulsory miss

Address (0000101100000 0 00)2 will have a compulsory miss

Address (0000110000000 0 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 16 bytes:

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address (000000010000 00 00)2 will have a compulsory miss

Address (000000100000 00 00)2 will have a compulsory miss

Address (000000110000 00 00)2 will have a compulsory miss

Address (000001000000 00 00)2 will have a compulsory miss

Address (000001010000 00 00)2 will have a compulsory miss

Address (000001100000 00 00)2 will have a compulsory miss

Address (000001110000 00 00)2 will have a compulsory miss

Address (000010000000 00 00)2 will have a compulsory miss

Address (000010010000 00 00)2 will have a compulsory miss

Address (000010100000 00 00)2 will have a compulsory miss

Address (000010110000 00 00)2 will have a compulsory miss

Address (000011000000 00 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 32 bytes:

2 offset byte bits; 3 bit for word offset; 11 bits for index; 16 bits for tag

Address (00000001000 000 00)2 will have a compulsory miss

Address (00000010000 000 00)2 will have a compulsory miss

Address (00000011000 000 00)2 will have a compulsory miss

Address (00000100000 000 00)2 will have a compulsory miss

Address (00000101000 000 00)2 will have a compulsory miss

Address (00000110000 000 00)2 will have a compulsory miss

Address (00000111000 000 00)2 will have a compulsory miss

Address (00001000000 000 00)2 will have a compulsory miss

Address (00001001000 000 00)2 will have a compulsory miss

Address (00001010000 000 00)2 will have a compulsory miss

Address (00001011000 000 00)2 will have a compulsory miss

Address (00001100000 000 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 64 bytes:

2 offset byte bits; 4 bit for word offset; 10 bits for index; 16 bits for tag

Address (0000000100 0000 00)2 will have a compulsory miss

Address (0000001000 0000 00)2 will have a compulsory miss

Address (0000001100 0000 00)2 will have a compulsory miss

Address (0000010000 0000 00)2 will have a compulsory miss

Address (0000010100 0000 00)2 will have a compulsory miss

Address (0000011000 0000 00)2 will have a compulsory miss

Address (0000011100 0000 00)2 will have a compulsory miss

Address (0000100000 0000 00)2 will have a compulsory miss

Address (0000100100 0000 00)2 will have a compulsory miss

Address (0000101000 0000 00)2 will have a compulsory miss

Address (0000101100 0000 00)2 will have a compulsory miss

Address (0000110000 0000 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =64; line size 128 bytes:

2 offset byte bits; 5 bit for word offset; 9 bits for index; 16 bits for tag

Address (000000010 00000 00)2 will have a compulsory miss

Address (000000100 00000 00)2 will have a compulsory miss

Address (000000110 00000 00)2 will have a compulsory miss

Address (000001000 00000 00)2 will have a compulsory miss

Address (000001010 00000 00)2 will have a compulsory miss

Address (000001100 00000 00)2 will have a compulsory miss

Address (000001110 00000 00)2 will have a compulsory miss

Address (000010000 00000 00)2 will have a compulsory miss

Address (000010010 00000 00)2 will have a compulsory miss

Address (000010100 00000 00)2 will have a compulsory miss

Address (000010110 00000 00)2 will have a compulsory miss

Address (000011000 00000 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

Second: Cache size varies from 1 to, steps of power 2, line size 16 bytes

1. Line size =16 bytes; Cache size= 1 KBs

2 offset byte bits; 2 bit for word offset; 6 bits for index; 22 bits for tag

Address (000000 010000 00 00)2 will have a compulsory miss

Address (000000 100000 00 00)2 will have a compulsory miss

Address (000000 110000 00 00)2 will have a compulsory miss

Address (000001 000000 00 00)2 will have a compulsory miss

Address (000001 010000 00 00)2 will have a conflict miss

Address (000001 100000 00 00)2 will have a conflict miss

Address (000001 110000 00 00)2 will have a conflict miss

Address (000010 000000 00 00)2 will have a conflict miss

Address (000010 010000 00 00)2 will have a conflict miss

Address (000010 100000 00 00)2 will have a conflict miss

Address (000010 110000 00 00)2 will have a conflict miss

Address (000011 000000 00 00)2 will have a conflict miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 2 KBs

2 offset byte bits; 2 bit for word offset; 7 bits for index; 21 bits for tag

Address (00000 0010000 00 00)2 will have a compulsory miss

Address (00000 0100000 00 00)2 will have a compulsory miss

Address (00000 0110000 00 00)2 will have a compulsory miss

Address (00000 1000000 00 00)2 will have a compulsory miss

Address (00000 1010000 00 00)2 will have a compulsory miss

Address (00000 1100000 00 00)2 will have a compulsory miss

Address (00000 1110000 00 00)2 will have a compulsory miss

Address (00001 0000000 00 00)2 will have a compulsory miss

Address (00001 0010000 00 00)2 will have a compulsory miss

Address (00001 0100000 00 00)2 will have a conflict miss

Address (00001 0110000 00 00)2 will have a conflict miss

Address (00001 1000000 00 00)2 will have a conflict miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 4 KBs

2 offset byte bits; 2 bit for word offset; 8 bits for index; 20 bits for tag

Address (0000 00010000 00 00)2 will have a compulsory miss

Address (0000 00100000 00 00)2 will have a compulsory miss

Address (0000 00110000 00 00)2 will have a compulsory miss

Address (0000 01000000 00 00)2 will have a compulsory miss

Address (0000 01010000 00 00)2 will have a compulsory miss

Address (0000 01100000 00 00)2 will have a compulsory miss

Address (0000 01110000 00 00)2 will have a compulsory miss

Address (0000 10000000 00 00)2 will have a compulsory miss

Address (0000 10010000 00 00)2 will have a compulsory miss

Address (0000 10100000 00 00)2 will have a compulsory miss

Address (0000 10110000 00 00)2 will have a compulsory miss

Address (0000 11000000 00 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 8 KBs

2 offset byte bits; 2 bit for word offset; 9 bits for index; 19 bits for tag

Address (000 000010000 00 00)2 will have a compulsory miss

Address (000 000100000 00 00)2 will have a compulsory miss

Address (000 000110000 00 00)2 will have a compulsory miss

Address (000 001000000 00 00)2 will have a compulsory miss

Address (000 001010000 00 00)2 will have a compulsory miss

Address (000 001100000 00 00)2 will have a compulsory miss

Address (000 001110000 00 00)2 will have a compulsory miss

Address (000 010000000 00 00)2 will have a compulsory miss

Address (000 010010000 00 00)2 will have a compulsory miss

Address (000 010100000 00 00)2 will have a compulsory miss

Address (000 010110000 00 00)2 will have a compulsory miss

Address (000 011000000 00 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 16 KBs

2 offset byte bits; 2 bit for word offset; 10 bits for index; 18 bits for tag

Address (00 0000010000 00 00)2 will have a compulsory miss

Address (00 0000100000 00 00)2 will have a compulsory miss

Address (00 0000110000 00 00)2 will have a compulsory miss

Address (00 0001000000 00 00)2 will have a compulsory miss

Address (00 0001010000 00 00)2 will have a compulsory miss

Address (00 0001100000 00 00)2 will have a compulsory miss

Address (00 0001110000 00 00)2 will have a compulsory miss

Address (00 0010000000 00 00)2 will have a compulsory miss

Address (00 0010010000 00 00)2 will have a compulsory miss

Address (00 0010100000 00 00)2 will have a compulsory miss

Address (00 0010110000 00 00)2 will have a compulsory miss

Address (00 0011000000 00 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 32 KBs

2 offset byte bits; 2 bit for word offset; 11 bits for index; 17 bits for tag

Address (0 00000010000 00 00)2 will have a compulsory miss

Address (0 00000100000 00 00)2 will have a compulsory miss

Address (0 00000110000 00 00)2 will have a compulsory miss

Address (0 00001000000 00 00)2 will have a compulsory miss

Address (0 00001010000 00 00)2 will have a compulsory miss

Address (0 00001100000 00 00)2 will have a compulsory miss

Address (0 00001110000 00 00)2 will have a compulsory miss

Address (0 00010000000 00 00)2 will have a compulsory miss

Address (0 00010010000 00 00)2 will have a compulsory miss

Address (0 00010100000 00 00)2 will have a compulsory miss

Address (0 00010110000 00 00)2 will have a compulsory miss

Address (0 00011000000 00 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Line size =16 bytes; Cache size= 64 KBs

2 offset byte bits; 2 bit for word offset; 12 bits for index; 16 bits for tag

Address ( 000000010000 00 00)2 will have a compulsory miss

Address ( 000000100000 00 00)2 will have a compulsory miss

Address ( 000000110000 00 00)2 will have a compulsory miss

Address ( 000001000000 00 00)2 will have a compulsory miss

Address ( 000001010000 00 00)2 will have a compulsory miss

Address ( 000001100000 00 00)2 will have a compulsory miss

Address ( 000001110000 00 00)2 will have a compulsory miss

Address ( 000010000000 00 00)2 will have a compulsory miss

Address ( 000010010000 00 00)2 will have a compulsory miss

Address ( 000010100000 00 00)2 will have a compulsory miss

Address ( 000010110000 00 00)2 will have a compulsory miss

Address ( 000011000000 00 00)2 will have a compulsory miss

So miss ratio= 12/12= 1

Proving that the cache works: Running the loop for 12 iterations instead of 1,000,000

**MemGen1 output addresses:**

addr 0: 0

addr 1: 1

addr 2: 2

addr 3: 3

addr 4: 4

addr 5: 5

addr 6: 6

addr 7: 7

addr 8: 8

addr 9: 9

addr 10: 10

addr 11: 11

*Experiment 2: Full Associative:*

First:

Line Size= 32 bytes; Random Replacement (when full cache); Cache Size varies from 1-16 Kbs:

1. cache size =1KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =2KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =4KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =8KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =16KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

Conclusion: because addresses are sequential till RAM size, the first of a 32-byte group will make a miss, while the other 31 will make hits, therefore for 1 M iterations: miss ratio = 1/line size = 1/32 = 0.03125

Second: Line Size= 32 bytes; Cache Size = 4 KB; Replacement way varies:

1. FIFO (first in first out when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. LRU (Least recently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. LFU (Least frequently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. Random (random replacement when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

Conclusion: because addresses are sequential till RAM size, the first of a 32-byte group will make a miss, while the other 31 will make hits,

When full, FIFO, LRU, LFU, random will have the same output.

Therefore for 1 M iterations and for all replacement ways: miss ratio = 1/line size= 1/32 = 0.03125

**MemGen2 output addresses:**

addr 0: 95291

addr 1: 41855

addr 2: 127388

addr 3: 87463

addr 4: 45196

addr 5: 35654

addr 6: 121437

addr 7: 119120

addr 8: 99577

addr 9: 56653

addr 10: 23189

addr 11: 18776

First:

Line Size= 32 bytes; Random Replacement (when full cache); Cache Size varies from 1-16 Kbs:

1. cache size =1KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =2KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =4KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =8KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =16KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

Conclusion: because addresses are random in range (0 to 128KB-1), therefore, changing the size will change the number of map lines mapped to the same cache line, and the number of bytes per line is not effective because of random addresses.

Therefore, miss ratio = 1-hit ratio = 1- cache size / RAM size = 1- cache size / 128 KB.

Second: Line Size= 32 bytes; Cache Size = 4 KB; Replacement way varies:

1. FIFO (first in first out when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. LRU (Least recently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. LFU (Least frequently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Random (random replacement when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (101110100001 11011)2 will have a compulsory miss

Address (010100011011 11111)2 will have a compulsory miss

Address (111110001100 11100)2 will have a compulsory miss

Address (101010101101 00111)2 will have a compulsory miss

Address (010110000100 01100)2 will have a compulsory miss

Address (010001011010 00110)2 will have a compulsory miss

Address (011101101001 01110)2 will have a compulsory miss

Address (111010001010 10000)2 will have a compulsory miss

Address (110000100111 11001)2 will have a compulsory miss

Address (011011101010 01101)2 will have a compulsory miss

Address (001011010100 10101)2 will have a compulsory miss

Address (001001001010 11000)2 will have a compulsory miss

So miss ratio= 12/12= 1

Conclusion: because addresses are random in range (0 to 128KB-1), therefore, changing the way of replacement and the number of bytes per line will not be effective because of random addresses.

Therefore, miss ratio = 1-hit ratio = 1- cache size / RAM size = 1- 4KB / 128 KB approximately = 0.96875.

**MemGen3 output addresses:**

addr 0: 53810273

addr 1: 37943413

addr 2: 6924328

addr 3: 27377853

addr 4: 22746943

addr 5: 34583200

addr 6: 45979746

addr 7: 56531887

addr 8: 40872586

addr 9: 65548770

addr 10: 23302519

addr 11: 64490723

First:

Line Size= 32 bytes; Random Replacement (when full cache); Cache Size varies from 1-16 Kbs:

1. cache size =1KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

1. cache size =2KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =4KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =8KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. cache size =16KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

Conclusion: because addresses are random in range (0 to 64MB), therefore, changing the size will change the number of map lines mapped to the same cache line, and the number of bytes per line is not effective because of random addresses.

Therefore, miss ratio = 1-hit ratio = 1- cache size / RAM size = 1- cache size / 64MB.

Second: Line Size= 32 bytes; Cache Size = 4 KB; Replacement way varies:

1. FIFO (first in first out when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. LRU (Least recently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. LFU (Least frequently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

1. Random (random replacement when cache full):

5 offset bits (Byte Select); 27 bits for tag

Address (1100110101 00010100011 00001)2 will have a compulsory miss

Address (1001000010 11111000011 10101)2 will have a compulsory miss

Address (0001101001 10101000001 01000)2 will have a compulsory miss

Address (0110100001 11000000101 11101)2 will have a compulsory miss

Address (0101011011 00010111001 11111)2 will have a compulsory miss

Address (1000001111 10110010101 00000)2 will have a compulsory miss

Address (1010111101 10011000011 00010)2 will have a compulsory miss

Address (1101011110 10011011101 01111)2 will have a compulsory miss

Address (1001101111 10101010100 01010)2 will have a compulsory miss

Address (1111101000 00110001111 00010)2 will have a compulsory miss

Address (0101100011 10010001011 10111)2 will have a compulsory miss

Address (1111011000 00001100111 00011)2 will have a compulsory miss

So miss ratio= 12/12= 1

Conclusion: because addresses are random in range (0 to 64 MB -1), therefore, changing the way of replacement and the number of bytes per line will not be effective because of random addresses.

Therefore, miss ratio = 1-hit ratio = 1- cache size / RAM size = 1- 4KB / 64 MB approximately = 0.99994.

**MemGen4 output addresses:**

addr 0: 0

addr 1: 1

addr 2: 2

addr 3: 3

addr 4: 4

addr 5: 5

addr 6: 6

addr 7: 7

addr 8: 8

addr 9: 9

addr 10: 10

addr 11: 11

First:

Line Size= 32 bytes; Random Replacement (when full cache); Cache Size varies from 1-16 Kbs:

1. cache size =1KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =2KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =4KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =8KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. cache size =16KB; line size 32 bytes:

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

Conclusion: because addresses are random in range (0 to 1024 B), therefore, RAM size <= Cache size. Therefore, all misses are compulsory.

Therefore, miss ratio = (RAM size / cache line size) / iterations = (1 KB / 32 B) / 1000000 = 3.2e-005.

Second: Line Size= 32 bytes; Cache Size = 4 KB; Replacement way varies:

1. FIFO (first in first out when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. LRU (Least recently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. LFU (Least frequently used replaced when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

1. Random (random replacement when cache full):

5 offset bits (Byte Select); 27 bits for tag

tag (0) will have a compulsory miss

next 11 tags also = 0, therefore 11 hits

So miss ratio= 1/12= 0.083333

Conclusion: because addresses are random in range (0 to 1024 B), therefore, RAM size <= Cache size. Therefore, all misses are compulsory.

Therefore, miss ratio = (RAM size / cache line size) / iterations = (1 KB / 32 B) / 1000000 = 3.2e-005.

**memGen5:** somewhat similar, conclusion at the end.

**memGen6:** LFU: since the first 128 (Cache size 4 KB / Line Size 32 bytes) addresses are placed in the cache when it’s empty and then each following address is a conflict miss that is placed in the first location in the cache, the first element will always be a miss, while the 127 other addresses that were stored in the first circulation will make hits. Since no. of iterations = 1000000 and 64 MB / 256 = 262144, therefore: no. of times to hit each of the stored 127 locations = 3. Therefore: no. of hits = 3\*127 = 381. Therefore: miss ratio for LFU = 1 - 381/1000000 = 0.999619.

For all other experiments, since line size < 512 (least possible line size to get a miss followed by a hit), therefore: miss percentage = 100%.

For direct mapping: since replacement rotates, therefore: miss percentage = 100%. Same for FIFO and LFU as it also rotates.

For random replacement: percentage for a hit = (1/262144) \* (1/1000000). therefore: miss percentage = 100%.

*Experiment 3: Set associative:*

The conclusions could be induced from direct mapped and full associative caches.

**Full conclusion**: (for memGen: 1, 4, 5): for sequential accesses that go: 0, 1, 2, …, pseudo RAM size-1, 0, 1, …

If (Cache size < pseudo RAM size)

Miss ratio = 1 / line size;

Else miss ratio = (pseudo RAM size / line size) / total number of accesses.

if random {

Miss ratio = 1- cache size / pseudo RAM size;

}